VOCAL

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VOCAL's embedded software libraries include a complete range of ETSI / ITU / IEEE compliant algorithms, in addition to many other standard and proprietary algorithms. Our software is optimized for execution on ANSI C and leading DSP architectures (TI, ADI, AMD, ARM, CEVA, LSI Logic ZSP, and MIPS). These libraries are modular and can be executed as a single task under a variety of operating systems or standalone with its own microkernel.

VOCAL has implemented various Error Correcting Algorithms to optimize power saving in many types of communications systems, including Wireless LANs, ADSL modems, VDSL modems, satellite systems, etc.

1. Turbo codes

The VOCAL implementation of Turbo Codes (TC) Forward Error Correcting (FEC) algoithms is available in several forms, including pure software and varying levels of hardware complexity utilizing UDI instructions. The Turbo Codes algorithms can be used on squared and non-squared QAM constellations and include both Full-Turbo coding and Multi-level Turbo Coding. The process of encoding is simpler than decoding; for this reason, this technique is very suitable for asymmetrical coding (where different coding is used in each direction of the communication system).

2. Low-Density-Parity-Check Codes

VOCAL's Low-Density-Parity-Check Codes (LDPC) Forward Error Correcting (FEC) algorithms are also available in several forms. These forms include pure software and varying levels of hardware complexity utilizing UDI instructions. Low-Density-Parity-Check Codes algorithms can be used on squared and non-squared QAM constellations and include both Full-Low-Density-Parity-Check Codes and Multi-level Low-Density-Parity-Check Codes. In this case, the process of decoding is simpler than encoding; therefore, this technique is also very suitable for asymmetrical coding.

3. Reed-Solomon (RS) coding

VOCAL Reed Solomon (RS) Forward Error Correcting (FEC) algorithms are available in several formats. These include pure software and varying levels of hardware complexity utilizing UDI instructions. The Reed Solomon algorithms rely on special properties of Galois Field (GF) operations. UDI instructions are recommended to support the efficient implementation of Galois Field operations. Where special assistive hardware is not available (as is the case on most general purpose processors), the algorithms are typically implemented via table look-ups or are performed in the log domain.

Optimization for specific architectures is available for varying levels of cache usage and processing power. Pure software solutions are available in several different forms for both the encoder and decoder. Different versions allow speed versus memory tradeoffs to be made, permitting efficient and easy expansion of the code for assembly language optimization.

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